

U.S. DEPARTMENT OF COMMERCE PATENT & TRADEMARK OFFICE

B/O Form PTO-1390		Transmittal Letter to the United States Designated/Elected Office (DO/EO/US) Concerning a Filing Under 35 USC 371		Attorney's Docket Number BALD3003/JEK U.S. Application Number of known
International Application Number PCT/EP00/03530		International Filing Date 19 April 2000		Priority Date Claimed 23 April 1999
Title of Invention PROTECTION OF THE CORE PART OF A COMPUTER AGAINST EXTERNAL MANIPULATION				
Applicant(s) for DO/EO/US Michael BALDISCHWEILER		Assignee		

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items under 35 USC 371:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 USC 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 USC 371.
3. ☒ This express request to begin national examination procedures (35 USC 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 USC 371(b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed 35 USC 371(c)(2).
 - a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
 - b. ☒ has been transmitted by the International Bureau.
 - c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ A translation of the International Application into English (35 USC 371(c)(2)).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 USC 371(c)(3))
 - a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
 - b. ☐ have been transmitted by the International Bureau.
 - c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
 - d. ☒ have not been made and will not be made.
8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 USC 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 USC 371(c)(4)). (☐ Executed ☒ Unexecuted)
10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 USC 371(c)(5)).

Items 11 to 16 below concern other document(s) or information included:

11. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☒ A **FIRST** preliminary amendment.
☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
14. ☐ A substitute specification.
15. ☐ A change of power of attorney and/or address letter.
16. ☒ Other items or information: 1 sheet formal drawings

Application Number (if Known) 09/926376		International Application Number PCT/EP00/03530		Attorney's Docket Number BALD3003/JEK	
				Calculations	PTO USE ONLY
17. The following fees are submitted: Basic National Fee (37 CFR 1.492(a)(1)-(5)): <input checked="" type="checkbox"/> Search report has been prepared by the EPO or JPO \$890.00 <input type="checkbox"/> International Preliminary Examination Fee paid to USPTO (37 CFR 1.482) \$710.00 <input type="checkbox"/> No International Preliminary Examination Fee paid to USPTO (37 CFR 1.482) but International Search Fee paid to USPTO (37 CFR 1.445(a)(2)) \$740.00 <input type="checkbox"/> Neither International Preliminary Examination Fee (37 CFR 1.482) nor International Search Fee (37 CFR 1.445(a)(2)) paid to USPTO \$1040.00 <input type="checkbox"/> International Preliminary Examination Fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4) \$100.00					
ENTER APPROPRIATE BASIC FEE AMOUNT				\$ 890.00	
Surcharge of \$130.00 for furnishing the oath or declaration later than <input type="checkbox"/> 20 <input type="checkbox"/> 30 months from the earliest claimed priority date (37 CFR 1.492(e)).					
CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total Claims	14 -20 =		× \$18.00		
Independent Claims	1 -3 =		× \$84.00		
Multiple Dependent Claims (if applicable)			+ \$280.00		
TOTAL OF ABOVE CALCULATIONS				\$ 890.00	
Reduction by ½ for filing by small entity, if applicable. Small Entity Status is asserted pursuant to 37 CFR 1.27 for this application.					
SUBTOTAL				\$ 890.00	
Processing fee of \$130.00 for furnishing the English translation later than <input type="checkbox"/> 20 <input type="checkbox"/> 30 months from the earliest claimed priority date (37 CFR 1.492(f)).					
TOTAL NATIONAL FEE				\$ 890.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). \$40.00 per property.					
TOTAL FEES ENCLOSED				\$ 890.00	
				Refunded:	
				Charged:	

a. ☒ A check in the amount of **\$890.00** to cover the fees is enclosed.

b. ☐ Please charge my **Deposit Account Number 02-0200** in the amount of \$_____ to cover the above fees.

A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to **Deposit Account Number 02-0200**. A duplicate copy of this sheet is enclosed.

Note: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.



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DATE: 23 October 2001

Respectfully submitted,

J. Ernest Kenney
 Attorney for Applicant

Registration Number: 19,179

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

International Patent Application
No. PCT/EP00/03530

PCT/DO/EO/US

International Filing Date: 19 April 2000

Attorney Docket: BALD3003/JEK

Applicant: Michael BALDISCHWEILER

For: PROTECTION OF THE CORE PART OF A COMPUTER AGAINST EXTERNAL
MANIPULATION

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Sir:

This Preliminary Amendment accompanies documents to establish the U.S. national stage processing of the above-identified international patent application. Before calculation of the filing fee and before examination, kindly amend the application as follows.

AMENDMENT

IN THE CLAIMS:

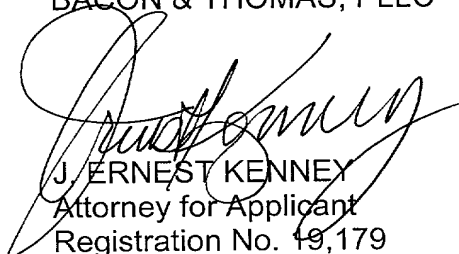
Please amend claims 1 - 14 as shown on the appended APPENDIX OF CLAIMS. Also appended hereto is an APPENDIX OF MARKED UP CLAIMS showing all of the revisions to the claims made by the present amendment.

International Application No. PCT/EP00/03530
Attorney Docket: BALD3003/JEK

REMARKS

Examination of the application as amended is respectfully requested.

Respectfully submitted,
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Date: October 23, 2001

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23364

PATENT TRADEMARK OFFICE

International Application No. PCT/EP00/03530
 Attorney Docket: BALD3003/JEK

APPENDIX OF CLAIMS

1(Amended). A method for protecting a computer with a central processing unit (CPU) from external manipulation, comprising: forming a final check sum by mathematical combination with reference to register contents of the CPU arising at the end of processing of an instruction by the CPU, and stored, and forming an initial check sum with reference to the register contents arising before the onset of processing of the next instruction by the CPU, and creating an error message if the initial check sum does not match the final check sum.

2(Amended). The method according to claim 1, wherein upon loading of the instruction a counter is started for counting the clock cycles necessary for executing the instruction and outputting an error signal when the predetermined clock cycles are overshoot or undershot.

3(Amended). The method according to claim 2, wherein the error signal triggers an interrupt or leads to discontinuance of the clock signal supply.

4(Amended). The method according to claim 1, wherein the number of clock cycles necessary for executing an instruction is obtained by a logic circuit from the opcode of the instruction.

5(Amended). The method according to claim 1, wherein the mathematical combination takes place by means of exclusive-OR combination of the register contents.

6(Amended). The method according to claim 1, wherein the initiation of the method is triggered by random or defined events.

7(Amended). The method according to claim 6, wherein the method is triggered in time-dependent fashion.

8(Amended). The method according to claim 6, wherein the method is triggered when the content of one or more registers of the CPU corresponds to a predetermined pattern.

9(Amended). The method according to claim 6, wherein the method is triggered after processing of a predetermined number of instructions in each case.

10(Amended). A central processing unit (CPU) for a computer for carrying out the method according to claim 1, comprising

- a combination of several registers of the CPU by logic elements to form a check sum,
- a check sum memory for storing a first check sum formed by the logic elements,
- a comparer for comparing a second check sum formed by the logic elements with the first check sum stored in the memory, and
- a control device for controlling the storage of the first check sum in the check sum memory and for controlling the comparer.

11(Amended). The central processing unit according to claim 10, including a counter for counting the clock cycles required for an instruction execution.

12(Amended). The central processing unit according to claim 10, including a logic circuit arranged to determine from the opcode of the instruction the clock cycles necessary for executing an instruction.

13(Amended). A computer comprising a central processing unit made according to claim 10.

14(Amended). A smart card comprising a central processing unit made according to claim 10.

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APPENDIX OF MARKED UP VERSION OF CLAIMS

1(Amended). A method for protecting a computer with a central processing unit (CPU) from external manipulation, [characterized in that] comprising: forming a final check sum [is formed] by mathematical combination with reference to register contents of the CPU arising at the end of processing of an instruction by the CPU, and stored, and forming an initial check sum [is formed] with reference to the register contents arising before the onset of processing of the next instruction by the CPU, and creating an error message [being effected] if the initial check sum does not match the final check sum.

2(Amended). [A] The method according to claim 1, [characterized in that] wherein upon loading of the instruction a counter is started for counting the clock cycles necessary for executing the instruction and outputting an error signal when the predetermined clock cycles are overshoot or undershot.

3(Amended). [A] The method according to claim 2, [characterized in that] wherein the error signal triggers an interrupt or leads to discontinuance of the clock signal supply.

4(Amended). [A] The method according to [any of claims 1 to 3, characterized in that] claim 1, wherein the number of clock cycles necessary for executing an instruction is obtained by a logic circuit from the opcode of the instruction.

5(Amended). [A] The method according to [any of claims 1 to 4, characterized in that] claim 1, wherein the mathematical combination takes place by means of exclusive-OR combination of the register contents.

6(Amended). [A] The method according to [any of claims 1 to 5, characterized in that] claim 1, wherein the initiation of the method is triggered by random or defined events.

7(Amended). [A] The method according to claim 6, [characterized in that] wherein the method is triggered in time-dependent fashion.

8(Amended). [A] The method according to claim 6, [characterized in that] wherein the method is triggered when the content of one or more registers of the CPU corresponds to a predetermined pattern.

9(Amended). [A] The method according to claim 6, [characterized in that] wherein the method is triggered after processing of a predetermined number of instructions in each case.

10(Amended). A central processing unit (CPU) for a computer for carrying out the method according to [any of claims 1 to 6] claim 1, comprising

- a combination of several registers of the CPU by logic elements to form a check sum,
- a check sum memory for storing a first check sum formed by the logic elements,
- a comparer for comparing a second check sum formed by the logic elements with the first check sum stored in the memory, and
- a control device for controlling the storage of the first check sum in the check sum memory and for controlling the comparer.

11(Amended). [A] The central processing unit according to claim 10, [characterized by] including a counter for counting the clock cycles required for an instruction execution.

12(Amended). [A] The central processing unit according to claim 10 [or 11], [characterized by] including a logic circuit [for determining] arranged to determine from the opcode of the instruction the clock cycles necessary for executing an instruction.

13(Amended). A computer comprising a central processing unit made according to [any of claims 10 to 12] claim 10.

14(Amended). A smart card comprising a central processing unit made according to [any of claims 10 to 12] claim 10.

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1/pv

Protection of a computer core from external manipulation

The present invention relates to the protection of a computer from external manipulation, in particular protection of the data present in the computer core or central processing unit (CPU). This invention is to be applied in particular for smart cards since they must be especially protected from manipulation from outside.

It is known to protect memory areas of a computer from manipulation for example by bus encryption, memory encryption and the like. DE 37 09 524 C2 discloses for example a test routine for checking the storage cell contents of a program memory. By forming a check sum over the storage cell contents at the onset of or during a program run and comparing it with a check sum previously stored in the program memory one can detect a change in the original storage cell contents as well as a change occurring only during operation, which leads to an error message.

The problem of the present invention is to propose a way of better protecting the computer from external manipulation.

This problem is solved according to the invention by a method, a central processing unit for carrying out said method, and a computer and smart card with such a central processing unit according to the features of the independent claims. Advantageous embodiments of the invention are stated in the subclaims.

The invention starts out from the idea of increasing the security of the computer by protecting the data present in the computer core, that is, in the central processing unit (CPU) of the computer, from external manipulation since the data are present in the computer core in unencrypted form and therefore easily manipulable.

In order to recognize such manipulation one determines a check sum from several register contents of the CPU by mathematical combination, for example by an exclusive-OR operation (XOR operation), after an instruction has been processed by the CPU and stores it in a memory as a final check sum. Before the next instruction is processed by the CPU a check sum is formed again, that is, the initial check sum. By comparing the initial check sum with the final check sum, which must match, one can ascertain whether register contents of the CPU were manipulated after the last instruction processing. As register contents one might use the contents of those

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areas of the CPU which can assume a nonzero state, such as in the 8051 type processor the accu, B-accu, data pointer (DPTR, DPL, DPH), registers (R0 to R7) of the register banks, program status word (PSW), stack pointer (SP), special function register (SPR) and the like.

To further increase security one can additionally, when loading an instruction, start a counter for counting the clock cycles necessary for executing the instruction. The counter is preferably constructed in terms of hardware. A logic derives from the instruction opcode the number of clock cycles necessary for execution and converts it into a counter value. The counter then runs parallel to the executed instruction. It is checked whether the instruction to be executed is executed within the stated clock cycles. In case the instruction was not executed within the predetermined time period, the clock supply is discontinued, for example, so that no further execution of instructions is possible. Alternatively a reset can be triggered and the central processing unit thus reset. The same steps can be taken if the instruction was executed prematurely, i.e. the limiting value of the instruction counter was not yet reached and a new operation code was already recognized.

The logical combination of the security-relevant registers can be realized by hardware or software. Check sum formation between two consecutive instructions can be effected for example on the basis of random or defined events or constantly.

The invention will be explained in more detail in the following with reference to the drawings, in which:

Fig. 1 shows the structure of a microcontroller by the example of an 8051 processor, and

Fig. 2 shows a logic for combining several areas of the central processing unit.

Fig. 1 shows the structure of an 8051 processor, that is, an 8-bit processor. While data are protected from manipulation by bus or memory encryption in known encryption methods, data are present in unencrypted form in the core of the computer, i.e. the central processing unit or CPU. The inventive method now determines whether one or more registers of the CPU have been manipulated.

Fig. 2 shows by way of example such security-relevant areas of the CPU that could be manipulated, namely stack pointer SP, accu AC, B-accu BAC, registers R0

to R7, data pointer DPL and DPH for the lower and upper areas of the internal RAM. Said registers are combined logically to form a check sum. In Fig. 2 two 8-bit registers are combined in each case by an exclusive-OR gate (XOR). Thus, XORing of registers R0 and R2 yields a new 8-bit pattern that is again XORed with the 8-bit pattern resulting from XORing of registers R1 and R7. Further XORing of the resulting 8-bit patterns finally yields an 8-bit pattern that serves as a check sum and is designated "initial check sum" in Fig. 2. Instead of XORing, which is advantageous in particular with respect to the effort, one can of course also choose other embodiments for forming the check sum.

If the combination of the registers is executed in terms of hardware by logic elements, the check sum changes immediately when the content of a register changes. That is, during execution of an instruction processed in the CPU the check sum might change many times. The only check sums crucial for carrying out the method, however, are the one after execution of an instruction and the one before execution of the next instruction since these two check sums (final check sum of one instruction and initial check sum of the next instruction) are compared in a comparer.

Comparison is performed as follows. The check sum arising at the end of execution of a first instruction is stored as the final check sum in a memory on the CPU. In order to ascertain whether manipulation of the CPU has taken place after execution of said first instruction and before loading of the next, second instruction into the CPU, the initial check sum is formed as described above parallel to the loading of said second instruction. In first step a) the initial check sum is compared by a comparer with the final check sum stored in the memory from the previously executed first instruction. In case no manipulation was performed on the CPU, the initial and final check sums match and the value of the result of comparison is zero. The comparer outputs a signal on the basis of which the currently available check sum is stored in the memory as the new final check sum in second step b) after execution of the second instruction. That is, the execution of the second instruction is not interrupted in this case. However, if comparison of the initial check sum and final check sum yields a nonzero value, manipulation of the CPU must be inferred.

The output signal of the comparer then leads not to second step b) but to error message c) which causes abortion of instruction processing in the case shown in Fig. 2. For example, the processor can be stopped, a security sensor activated or, in the case of a smart card, the smart card withheld by the terminal.

The above-described security mechanism can also be realized strictly in terms of software by the check sums being determined at the end of an instruction execution, on the one hand, and at the onset of the next instruction execution, on the other hand, and compared. The corresponding program can be stored for example in the ROM or EPROM of the processor and the final check sum stored in the bit-addressable RAM of the processor.

The described method need not be performed before each instruction to be executed. One embodiment of the invention provides for the carrying out of the method to depend on a random or defined event. According to a first embodiment, the method can be triggered in time-dependent fashion.

According to another embodiment, the method can be triggered by the content of one or more registers of the CPU corresponding to a predetermined pattern.

Yet another embodiment of the invention provides for the method to be triggered after processing of a predetermined number of instructions in each case.

A preferred embodiment is one by which the method is only triggered if there is a relatively long, defined time period between the instruction after whose execution the check sum was stored as the final check sum in the memory and the initial check sum at the onset of execution of the next instruction. This saves valuable computer capacity in execution of a program with many instructions. Assuming that manipulation of the CPU, in particular with smart cards, does not take place during the program run but when the smart card is removed from the smart card terminal, manipulation of the CPU is nevertheless reliably detectable by means of this latter described embodiment.

Patent claims

1. A method for protecting a computer with a central processing unit (CPU) from external manipulation, characterized in that a final check sum is formed by mathematical combination with reference to register contents of the CPU arising at the end of processing of an instruction by the CPU, and stored, and an initial check sum is formed with reference to the register contents arising before the onset of processing of the next instruction by the CPU, an error message being effected if the initial check sum does not match the final check sum.
2. A method according to claim 1, characterized in that upon loading of the instruction a counter is started for counting the clock cycles necessary for executing the instruction and outputting an error signal when the predetermined clock cycles are overshoot or undershot.
3. A method according to claim 2, characterized in that the error signal triggers an interrupt or leads to discontinuance of the clock signal supply.
4. A method according to any of claims 1 to 3, characterized in that the number of clock cycles necessary for executing an instruction is obtained by a logic circuit from the opcode of the instruction.
5. A method according to any of claims 1 to 4, characterized in that the mathematical combination takes place by means of exclusive-OR combination of the register contents.
6. A method according to any of claims 1 to 5, characterized in that the initiation of the method is triggered by random or defined events.
7. A method according to claim 6, characterized in that the method is triggered in time-dependent fashion.
8. A method according to claim 6, characterized in that the method is triggered when the content of one or more registers of the CPU corresponds to a predetermined pattern.
9. A method according to claim 6, characterized in that the method is triggered after processing of a predetermined number of instructions in each case.

10. A central processing unit (CPU) for a computer for carrying out the method according to any of claims 1 to 6, comprising
 - a combination of several registers of the CPU by logic elements to form a check sum,
 - a check sum memory for storing a first check sum formed by the logic elements,
 - a comparer for comparing a second check sum formed by the logic elements with the first check sum stored in the memory, and
 - a control device for controlling the storage of the first check sum in the check sum memory and for controlling the comparer.
11. A central processing unit according to claim 10, characterized by a counter for counting the clock cycles required for an instruction execution.
12. A central processing unit according to claim 10 or 11, characterized by a logic circuit for determining from the opcode of the instruction the clock cycles necessary for executing an instruction.
13. A computer comprising a central processing unit according to any of claims 10 to 12.
14. A smart card comprising a central processing unit according to any of claims 10 to 12.

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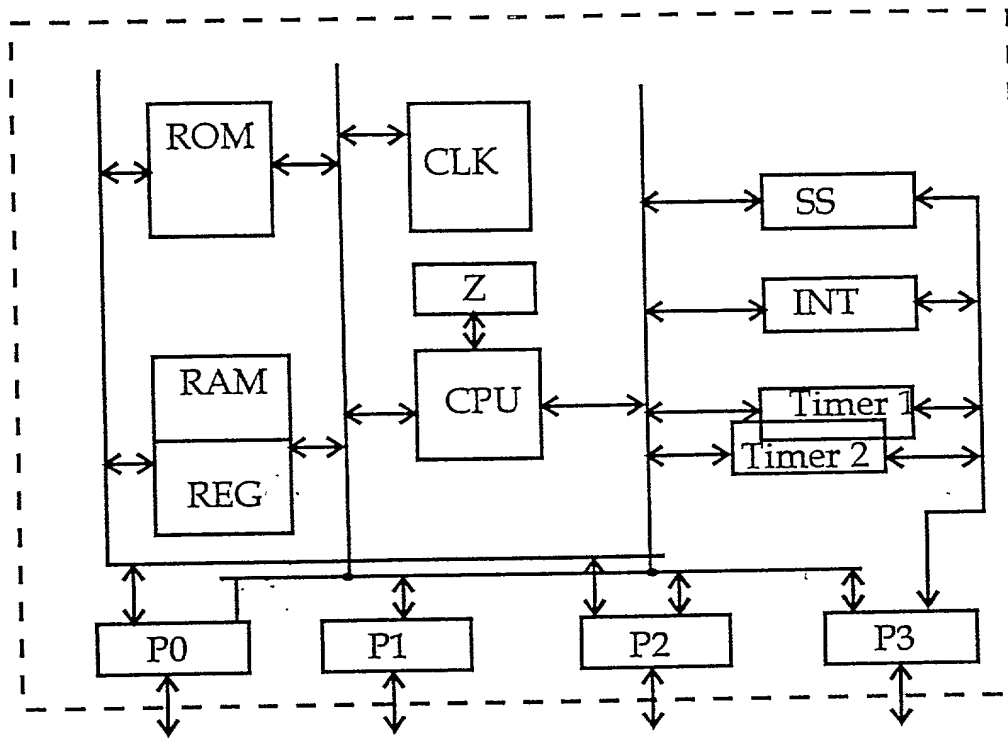


Fig. 1

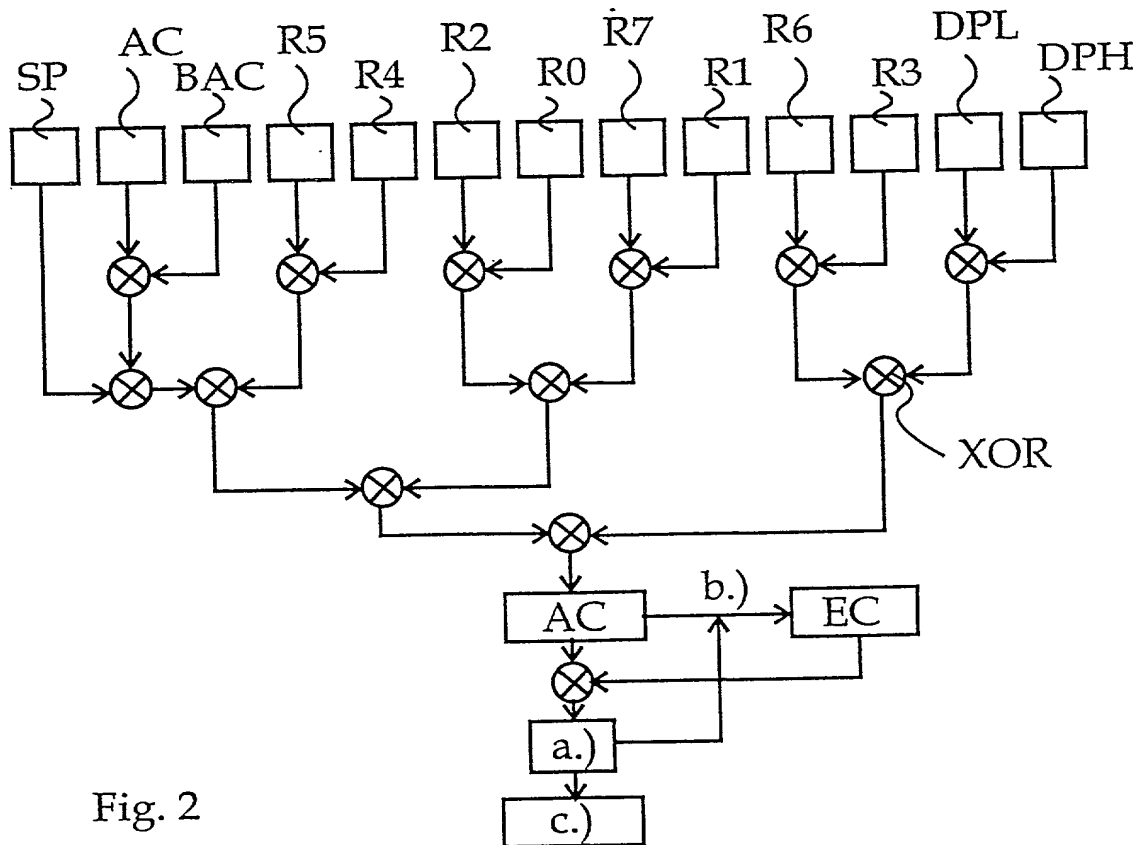


Fig. 2

DECLARATION FOR PATENT APPLICATION AND APPOINTMENT OF ATTORNEY

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name; I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention (Design, if applicable) entitled: **PROTECTION OF THE CORE PART OF A COMPUTER AGAINST EXTERNAL MANIPULATION** the specification of which (check one):

☐ is attached hereto, or ☒ was filed on: **19 April 2000**
International Application Number: **(PCT/EP00/03530) 09/926.376**

as U.S. Application Number or PCT
and (if applicable) was amended on:

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above. I acknowledge the duty to disclose information which is material to patentability as defined in *Title 37, Code of Federal Regulations, §1.56*. I hereby claim foreign priority benefits under *Title 35, United States Code §119* of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

PRIOR FOREIGN APPLICATION(S)			PRIORITY CLAIMED	
Number	Country	Day/Month/Year Filed	Yes	No
199 18 620.0	Germany ✓	23 April 1999 ✓	X	

☐ Additional Priority Application(s) Listed on Following Page(s)

I HEREBY CLAIM THE BENEFIT UNDER TITLE 35 U.S. CODE §119(E) OF ANY U.S. PROVISIONAL APPLICATIONS LISTED BELOW.	
Application Number	Day/Month/Year Filed

☐ Additional Provisional Application(s) Listed on Following Page(s)

I hereby claim the benefit under *Title 35, United States Code, §120* of any United States application(s) or PCT international application(s) designating The United States of America listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of *Title 35, United States Code, §112*, I acknowledge the duty to disclose information which is material to patentability as defined in *Title 37, Code of Federal Regulations, §1.56* which became available between the filing date of the prior application(s) and the national or PCT international filing date of this application:

Application Number	Filing Date	Status - Patented, Pending or Abandoned

☐ Additional US/PCT Priority Application(s) listed on Following Page(s)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under *section 1001 of title 18 of the United States Code* and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: I (We) hereby appoint as my (our) attorneys, with full powers of substitution and revocation, to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: J. Ernest Kenney, Reg. No. 19,179; Eugene Mar, Reg. No. 25,893; Richard E. Fichter, Reg. No. 26,382; Thomas J. Moore, Reg. No. 28,974; Joseph DeBenedictis, Reg. No. 28,502; Benjamin E. Urcia, Reg. No. 33,805; and

I (we) authorize my (our) attorneys to accept and follow instructions from Klunker, Schmitt-Nilson, Hirsch regarding any matter related to the preparation, examination, grant and maintenance of this application, any continuation, continuation-in-part or divisional based thereon, and any patent resulting therefrom, until I (we) or my (our) assigns withdraw this authorization in writing.

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FULL NAME OF FIRST OR SOLE INVENTOR Michael BALDISCHWEILER	CITIZENSHIP Germany ✓
RESIDENCE ADDRESS Friedrich-Eckardstr. 60, D-81929 Munchen Germany DEX	POST OFFICE ADDRESS IS THE SAME AS RESIDENCE ADDRESS UNLESS OTHERWISE SHOWN BELOW
DATE München 9.11.2001	SIGNATURE X Michael Baldischweiler

☐ See following page(s) for additional joint inventors.